Compact modeling of external parasitics of graphene field-effect transistors

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Abstract

Graphene is a promising candidate for future high-performance RF applications [1]. Its potential to substitute conventional silicon technology has been demonstrated with devices such as a graphene field-effect transistor (GFET) with an intrinsic cut-off frequency of 427 GHz [2]. Recently, research on graphene-based RF electronics has been extended to the circuit level and basic building blocks such as mixers [3] and amplifiers [4] have been reported. This scenario leads to a demand for accurate compact models for circuit design engineers. These models have to cover not only the intrinsic device, but also the bias-dependent and performance-degrading extrinsic elements.

In this work we develop a compact model of the extrinsic part of a typical GFET structure. It is implemented in Verilog-A and usable with conventional circuit simulators. We assume a double-gate GFET structure with a channel of pristine monolayer graphene (Fig. 1). The intrinsic channel is covered by a high- κ /metal gate stack and modeled such as proposed in [5]. The extrinsic model consists of the contact resistances R_{m-g} and R_{g-c} at the metal-graphene interface, the access resistance R_c of the graphene contact layer between the electrodes and the intrinsic device, and fringe capacitances $C_{c,x}$ between the electrodes and this graphene layer (Fig. 2).

 R_{m-g} and R_{g-c} are due to two consecutive tunneling processes at the metal-graphene interface. In compact models these resistances have up to now been empirically approximated [6, 7]. We implemented them following the description of the underlying physical processes given in [8] and using a combination of power-law and linear curve fitting (Fig. 3). R_c is due to the finite resistance of the extrinsic graphene layer. In a novel approach we split this region into segments and consider each of them as an individual triple-gate GFET device, which is weakly coupled to the gate and source/drain electrodes as well as to the back-gate (Figs. 4 and 5). There is a low voltage drop over the individual segments, which implies Fermi-levels close to the Dirac point. We have developed a drain current description which is accurate under these low-voltage conditions and have validated it by comparison to experiments [9] (Fig. 6).

Simulations show that the extrinsic resistances have a strong impact on device current I_d (Fig. 7). When simply regarding the intrinsic device, a variation of the back-gate voltage V_{bs} only leads to a shift in the point of minimum current. By considering R_{m-g} , R_{g-c} , and R_c , a decrease in I_d can be observed. An efficient method to mitigate these parasitic resistances is to induce additional charge carriers in the extrinsic graphene layer by increasing V_{bs} (Fig. 8). For instance, a change in V_{bs} from 0 to 20 V yields a decrease of the overall contact resistance from 5.49 to 2.18 k $\Omega \cdot \mu m$. These high V_{bs} values have been obtained for a back-gate oxide thickness of 300 nm. V_{bs} could be strongly reduced by for instance using a state-ofthe-art FDSOI oxide thickness of 25 nm.

Based on these results, our work indicates the need for accurately modeling the GFET's external resistances. Furthermore, applying a back-gate potential allows to significantly reduce them.

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^{*} G.M. Landauer acknowledges the support of an FI grant of the Government of Catalonia and the European Social Fund as well as the support of the Spanish Ministry of Science and Innovation under project TEC2008-01856 with additional participation of FEDER funds. ** D. Jiménez acknowledges funding from the Ministerio de Economía y Competitividad of Spain under the project TEC2012-31330, and from the

^{**} D. Jimenez acknowledges funding from the Ministerio de Economía y Competitividad of Spain under the project TEC2012-31330, and from the European Union Seventh Framework Programme under grant agreement nº604391 Graphene Flagship.

Figures







Fig. 3: Contact resistance $R_{m-g} + R_{g-c}$ at the metal-graphene interface vs. Fermi levels E_{fm} and E_{ig} under the metal electrode and at the beginning of the extrinsic graphene contact layer, respectively. Curve fitting is used.



Fig. 5: Segment-to-electrode outer-fringe capacitance $C_{c,x}$ for a geometry with $L_c = L_g = L_s = L_d = 1 \ \mu m$ and 100 nm contact height. Results were obtained with an EM field simulator and implemented in the model using power-law fitting.







Fig. 2: Equivalent circuit of the GFET showing extrinsic resistances and capacitances. The distributed model of the graphene contact layer is shown in a symbolized form.



Fig. 4: Splitting of the graphene contact layer into *N* segments. Each one is described as an individual weakly coupled GFET and modeled with high accuracy at low voltage drops.



Fig. 6: Low-voltage GFET model with high accuracy close to the Dirac point. A validation against measurement data for V_{ds} = 10 mV [9] shows a gain in accuracy close to the point of minimum current when comparing to previous models [5], [10].



